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Design Overview of the Electronics and Front-End Data Acquisition System for the Outer Veto

Introduction

This document is intended to provide a brief overview of the electronic system that is envisioned for the outer veto system. It is based on the concept of a digital readout in which no analog information from the detectors is recorded. The digital responses of individual detectors (hit or not-hit) are bit-packed into a single word for each module. In addition, some very preliminary estimates of data rates are provided. These estimates are based on early observations in the cosmic-ray test stand at Argonne and the muon rate simulations which have been shown at collaboration meetings.

Detector Overview

The Outer Veto system will consist of individual modules of gas filled long-tube wire proportional chambers. The modules will be constructed in a 8 wide by 3 deep close-packed configuration. Electronic connection to the module will be made via two threaded brass posts for each individual chamber (tube): one in contact with the crimped wire and the other providing the return current connection to the outer tube.

These modules will be assembled into square, flat panels by placing modules side-by-side and then placing two of these groups together orthogonally. In the near detector laboratory, each group will consist of 13 side-by-side 5.3 meter long modules while in the far detector, each group will consist of 17 side-by-side 6.8 meter long modules. The near detector will require 10 of these panels for a total of 260 modules or 6240 total channels. Due to physical constraints, the far detector will only allow 2 panels for a total of 68 modules or 1632 total channels.

Front-End Electronics

We foresee a single printed circuit board which will be placed on one end of each module. The board will connect to the threaded brass connections provided by the mechanical construction of each tube. A single high-voltage connection will supply all chambers in that module. The analog signal from each wire will be read-out and immediately put into a discriminator which operates in time-over-threshold mode with a 10MHz clock (ie. digitized every 100ns). This discriminated signal will be passed into an FPGA on the front-end card which will compile the output from all 24 chambers into a single 24-bit data word. When a trigger condition is satisfied, a 24-bit timestamp will be appended to each 24-bit encoded data word and it will be sent through a hot-link connection to the back-end VME system. We foresee the following three trigger conditions:

1) **Simple Coincidence**: Since any muon will have greater than a 99% chance of causing a signal in at least 2 out of 3 chambers within a single module, this will provide the most effective method for reducing the random singles rate while maintaining a very high efficiency of muon detection. In order to avoid missing events which may span a clock boundary, we propose to use a simple sliding window of two clock cycles which will be used to define a coincidence.
2) **Long Pulse Trigger**: A showering muon may have multiple particles interacting in a single chamber over a period of time up to 1-2μs. For that reason, the data for a channel which is above threshold for contiguous clock-cycles will be stored. If the simple coincidence described above is satisfied at any time during the contiguous period, all digits for the contiguous period will be sent to the back-end system.

3) **Diagnostic Trigger**: For calibration or debugging purposes, a special trigger will be available. In this configuration, if any of the 24 channels are above threshold, the 24-bit data word will be triggered and sent to the back-end system. Since this will have a high rate, this is foreseen as a configurable trigger condition.

Additionally, the front-end board will allow communication from the VME system. This will be required to modify the trigger configurations as specified above as well as allowing the ability to mask off channels that have gone bad. Since the performance of the tubes is very uniform, it is foreseen to only have a single tunable discriminator threshold applied to all of the 24 channels in a module.

Back-End System

The back-end is expected to be based on a single VME 9U crate at each detector location. Communication between the front-end and back-end will be done serially with the use of fiber-optic cables, to reduce the possibility of ground loops. It is hoped that small fiber-optic connectors can be found which will allow 16 front-end modules to communicate to a single back-end VME card. At that density, the 260 modules of the near detector could fit in 17 modules within a single crate. The VME modules will consist of independent data channels for each input channel. The data will have address and control codes appended and will be stored in dual-port buffers. The VME processor will be used to readout the data via dma block transfer on a periodic basis (perhaps once or twice per second?). Once in the VME processor, the data can be assembled into any desirable format for the full DAQ to receive.

Timing System

This still needs to be defined. It is perhaps possible to have a synchronized timestamp between the main DAQ and the VME processor. Additionally, the timing system will have to provide a distributed 10 MHz clock to all front-end boards and provide a periodic signal for the readout of the VME system.

Expected Data Rates

As a worst-case, we consider that an individual module can have up to 500Hz random singles. At that rate, the simple coincidence trigger would get something like 1-2 Hz of readout. The muon signal rate, however, is expected to be approximately 30 Hz per module on average across the near detector laboratory. Most muon signals are relatively short and would be entirely contained within a single clock cycle, however approximately 10% of the muon signals have been observed to be large – spanning as much as 1.5μs. For a conservative estimate, we assume that an individual module will present a trigger rate of 100 Hz in which 10% are of 1μs duration. That yields the following maximum data rates:

Number of Events /module (Event = single clock-cycle digitization which is triggered)	190 events/s
Serial Output Bit Rate per module (24 data bits + 24 timestamp + 1 header and trailer /byte)	11,400 bits/s
Back-End Output Rate per Card (16 Module Inputs/Card) (assume location Id and informative flags are appended to 48-bit data to produce 64-bit word for each stored event)	24,320 bytes/s
Combined Data Output Rate (17 Cards in Near Detector) (5 Cards in the Far Detector)	413,440 bytes/s 121,600 bytes/s
Total data flow rate (both detectors)	46.2 Gbytes/day