Double Chooz Outer Veto
Front-end Electronics
U of C EDG

64 Fibers → PMT 64 → Preamp → Comparator → Shaper → Sample & Hold → ADC → To FPGA

Gain Control → Reference DAC

Memory (if needed) → ADC Buffer

DC to DC HV Converter

FPGA → Transparent Buffer → ADC Buffer → 2 Port Memory → Multiplexer → Parallel to Serial Driver → Trigger Out

2 Port Memory

Control Signals from Master

Clock & Control Distribution

Control & Time Signals